			Spartan-6 LX FPGAs Optimized for Lowest-Cost Logic, DSP, and Memory (1.2V, 1.0V)								Spartan-6 LXT FPGAs Optimized for Lowest-Cost Logic, DSP, and Memory with High-Speed Serial Connectivity (1.2V)				
	Part Number		XC6SLX4	XC6SLX9	XC6SLX16	XC6SLX25	XC6SLX45	XC6SLX75	XC6SLX100	XC6SLX150	XC6SLX25T	XC6SLX45T	XC6SLX75T	XC6SLX100T	XC6SLX150T
Logic Resources	Slices[1]		600	1,430	2,278	3,758	6,822	11,662	15,822	23,038	3,758	6,822	11,662	15,822	23,038
	Logic Cells[2]		3,840	9,152	14,579	24,051	43,661	74,637	101,261	147,443	24,051	43,661	74,637	101,261	147,443
	CLB Flip-Flops		4,800	11,440	18,224	30,064	54,576	93,296	126,576	184,304	30,064	54,576	93,296	126,576	184,304
Memory Resources	Maximum Distributed RAM (Kb)		75	90	136	229	401	692	976	1,355	229	401	692	976	1,355
	Block RAM (18 Kb each)		12	32	32	52	116	172	268	268	52	116	172	268	268
	Total Block RAM (Kb)[3]		216	576	576	936	2,088	3,096	4,824	4,824	936	2,088	3,096	4,824	4,824
Clock Resources	Clock Management Tiles (CMT)[4]		2	2	2	2	4	6	6	6	2	4	6	6	6
I/O Resources	Maximum Single-Ended Pins		132	200	232	266	358	408	480	576	250	296	348	498	540
	Maximum Differential Pairs		66	100	116	133	179	204	240	288	125	148	174	249	270
Embedded Hard IP Resources	DSP48A1 Slices[5]		8	16	32	38	58	132	180	180	38	58	132	180	180
	Endpoint Block for PCI Express®		—	—	—	—	—	—	—	—	1	1	1	1	1
	Memory Controller Blocks		0	2	2	2	2	4	4	4	2	2	4	4	4
	GTP Low-Power Transceivers		—	—	—	—	—	—	—	—	2	4	8	8	8
Speed Grades	Commercial[10]		-1L, -2, -3	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N
	Industrial[10]		-1L, -2, -3	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N
Configuration	Configuration Memory (Mb)		2.7	2.7	3.7	6.4	11.9	19.6	26.5	33.8	6.4	11.9	19.6	26.5	33.8
	Package	Body Area	Maximum User I/O: SelectIO™ Interface Pins (GTP Transceivers)[6]												
	Chip Scale Packages (CPG): Pb-free, wire-bond, chip scale BGA (0.5 mm ball spacing)														
	CPG196[7]	8 x 8 mm	106	106	106										
	TQFP Packages (TQG): Pb-free, thin QFP (0.5 mm lead spacing)														
	TQG144[7]	20 x 20 mm	102	102											
	Chip Scale Packages (CSG): Pb-free, wire-bond, chip scale BGA (0.8 mm ball spacing)														
	CSG225[8]	13 x 13 mm	132	160	160										
	CSG324	15 x 15 mm		200	232	226	218				190 (2)	190 (4)			
	CSG484[9]	19 x 19 mm					320	328	338	338		296 (4)	292 (4)	296 (4)	296 (4)
	BGA Packages (FTG): Pb and Pb-free, wire-bond, fine-pitch thin BGA (1.0 mm ball spacing)														
	FT(G)256	17 x 17 mm		186	186	186									
	BGA Packages (FGG): Pb and Pb-free, wire-bond, fine-pitch BGA (1.0 mm ball spacing)														
	FG(G)484[9]	23 x 23 mm				266	316	280	326	338	250 (2)	296 (4)	268 (4)	296 (4)	296 (4)
	FG(G)676	27 x 27 mm					358	408	480	498			348 (8)	376 (8)	396 (8)
	FG(G)900	31 x 31 mm								576				498 (8)	540 (8)

XMP071 (v1.2)

Notes:
1. Each slice contains four LUTs and eight flip-flops.
2. Spartan-6 FPGA logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT architecture.
3. Block RAM are fundamentally 18Kb in size. Each block can also be used as two independent 9 Kb blocks.
4. Each CMT contains two DCMs and one PLL.
5. Each DSP48A1 slice contains an 18x18 multiplier, an adder, and an accumulator.
6. The LX device pinouts are not compatible with the LXT device pinouts.
7. CPG196 and TQG144 do not have memory controller support. -3N is not available for these packages.
8. CSG225 has X8 memory controller support in the LX9 and LX16 devices. There is no memory controller in the LX4 devices.
9. Devices in the FG(G)484 and CSG484 packages have support for two memory controllers.
10. Devices with -3N speed grade do not support MCB functionality

Important: Verify all data in this document with the device data sheets found at www.xilinx.com